



Silicon Valley Technical Institute

1762 Technology Drive

San Jose, CA

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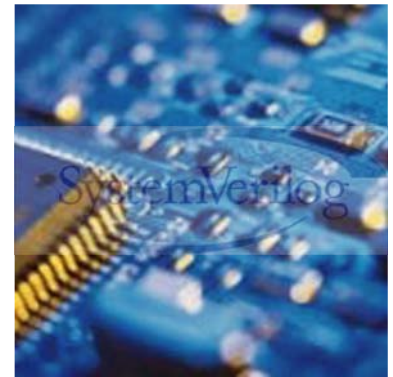
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Practical Application of the Verification Methodology Manual (VMM) Using SystemVerilog

TBD
9am-5pm

"Practical Application of the Verification Methodology Manual (VMM) is a 2-day comprehensive training workshop that teaches how to write a SystemVerilog transaction-based testbench compliant to the "Verification Methodology Manual for SystemVerilog" (VMM) by Janick Bergeron, et. al.. The VMM provides the details of a powerful methodology, but the VMM is not a tutorial. This workshop fills that gap, teaching how to apply the VMM concepts in a practical, realistic design environment. A FIFO design and a serial-to-parallel design are used to illustrate using the VMM methodology for the creation of a comprehensive constrained-random verification environment. Labs reinforce these VMM concepts. Students receive a comprehensive training guide that will serve as an invaluable aid in applying the concepts in the VMM. Major topics presented in this workshop include:



- **The generation of, and the consumption of, transactions via transactors**
- **The definition of the verification environment**
- **Using the VMM monitor class**
- **Using the VMM scoreboard class**
- **Using VMM factory and callback methods**
- **Directed tests**
- **The VMM custom aenerator**

This workshop is for verification engineers who are already familiar with Verilog and the SystemVerilog testbench constructs.

About the Instructor:

Ben Cohen is an HDL and property languages (PSL, SystemVerilog Assertions) trainer and consultant. He has technical experience in digital and analog hardware design, computer architecture, ASIC design, synthesis, and use of hardware description languages for modeling of statistical simulations, instruction set descriptions, and hardware models. He is the author of several books on VHDL, PSL, SVA and design verification.

Schedule

Check-in: 8:30 am –9:00 am

Lecture: 9:00 am - 5.00 pm

Lunch: noon-1:00 pm

Tuition

Fee for the seminar is **\$1200**. The registration fee includes:

- Two days of instruction
- Seminar notes

Location

Silicon Valley Technical Institute, 1762 Technology Drive, STE 227, San Jose, CA

Seating is limited.
Please register in advance.
Register on line by [clicking here](#) or
Call: 408-573-0100