



Silicon Valley Technical Institute

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SystemVerilog Testbench for Verification Engineers

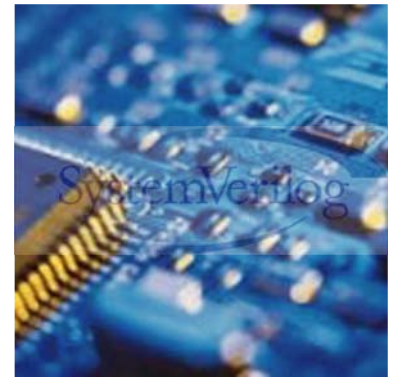
TBD

9am-5pm

"SystemVerilog Testbench for Verification Engineers" is a 2-day fast-paced workshop covering the testbench constructs in the IEEE 1800-2005 SystemVerilog standard. SystemVerilog unifies the strengths of Verilog, VHDL, C, VERA and PSL in one language, making it a true "HDVL", or "Hardware Description and Verification Language". SystemVerilog enables the verification of very large, complex designs using a single language for all aspects of the design cycle, including simulation, synthesis and formal verification. The focus of "SystemVerilog Testbench for Verification Engineers" is on the verification aspects of SystemVerilog. Concepts presented include new special testbench modeling constructs, defining clocking domains, and avoiding simulation race conditions. Several labs reinforce the principles presented, with forty percent of the class time devoted to hands-on experience. Just a few of the SystemVerilog verification constructs that are presented include:

- **Specifying and using dynamic arrays**
- **SystemVerilog dynamic processes**
- **Object Oriented verification**
- **Using mailboxes and semaphores**
- **Constrained random test generation**
- **Defining and using functional coverage**

The course presupposes a working knowledge of Verilog, and only covers the SystemVerilog testbench enhancements to Verilog.



About the Instructor:

Stuart Sutherland is the founder and a principal engineer of Sutherland HDL, Inc., where he provides expert SystemVerilog design services, and presents advanced level training workshops. He brings more than 20 years of experience in hardware design, and over 16 years experience with Verilog to the classroom. He is co-author of the book "SystemVerilog for Design Engineers", and is the author of "The Verilog PLI Handbook", and the popular "Verilog HDL Quick Reference Guide" and "Verilog PLI Quick Reference Guide".

Schedule

Check-in: 8:30 am –9:00 am

Lecture: 9:00 am - 5.00 pm

Lunch: noon-1:00 pm

Tuition

Fee for the seminar is **\$1200**. The registration fee includes:

- Two days of instruction
- Seminar notes

Location

Silicon Valley Technical Institute, 1762 Technology Drive, STE 227, San Jose, CA

Seating is limited.
Please register in advance.
Register on line by clicking here or
Call: 408-573-0100