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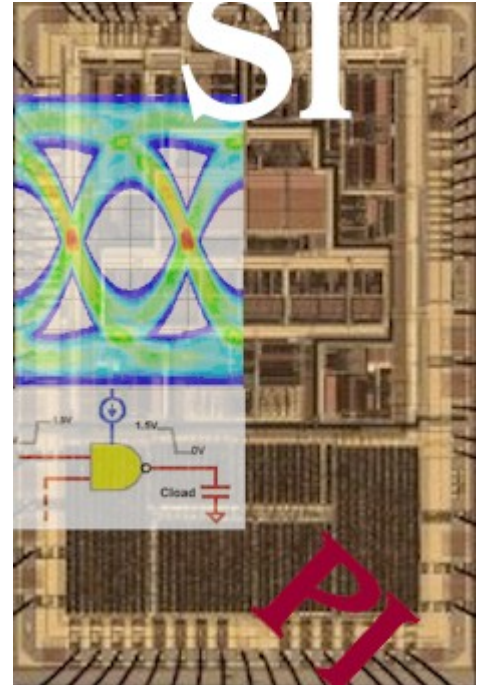
SIGNAL INTEGRITY/NOISE ISSUES IN NANOMETER VLSI/SOC DESIGNS

Oct. 26, 2007

9am-4:30pm

Signal Integrity (SI) is a major topic in high-speed digital VLSI/SoC designs, and an increasing challenge to design engineers. It refers to the ability to maintain the timing and quality of digital signals as they propagate throughout the circuit. The scope of SI has been expanded over time to include topics such as Power Integrity (e.g. IR drop, etc.), functional noise analysis, and analysis of the noise effect on timing. As signal integrity analysis tools become commonplace, the need for viable methodologies and solutions, addressing these critical issues, is more pressing than ever. Increased emphasis on low power designs, along with migration to smaller semiconductor processes creates even more challenges to overcome. This one-day seminar is intended for design engineers involved with design of digital VLSI circuits, and aims to explore the topics outlined below:

- **Definitions**
- **SI Importance**
- **Functional SI or noise glitch analysis**
- **Delay SI or noise effect on timing**
- **Voltage-variation impact and IR drop analysis**
- **Real world consequences of inaccurate delay calculation**
- **Variable current source modeling**
- **SI for low-power designs**
- **SI analysis challenges for 65 nanometer and below**
- **Emerging SI analysis approaches**



Schedule

Check-in: 8:30 am –9:00 am

Lecture: 9:00 am - 4.00 pm

Lunch: noon-1:00 pm

Tuition

Fee for the seminar is **\$370**. Group discount is available for groups of 3 or larger. The registration fee includes:

- One day of instruction
- Seminar notes
- Certificate

Lunch and refreshments are also provided

Location

1762 Technology Drive, Suite 227, San Jose, CA

About the Instructor:

Rahul Deokar is the product marketing director for Encounter digital IC design at Cadence Design Systems, Inc. with focus on digital timing, and signal integrity including variability and manufacturability effects. Prior to Cadence, Deokar worked in R&D on timing analysis and logic/physical synthesis at Ambit Design Systems. Before working at Ambit, he was in the advanced R&D team at Bell Laboratories, Lucent Technologies. Rahul Deokar received an MS (Computer Engineering) from Iowa State University and an M.B.A from Santa Clara University.

Seating is limited.
Please register in advance.
Register on line at
<http://www.svtii.com> or
Call: 408-573-0100