



# Silicon Valley Technical Institute

1762 Technology Drive

San Jose, Ca

Tel: 408-573-0100

[www.svtii.com](http://www.svtii.com)

## Mixed- Signal VLSI/SoC Test

Feb. 04, 2005

9am-4pm

Today's mixed-signal VLSI chips contain digital logic, memory, and analog functions. Test procedures for these three types of functions differ and their understanding is essential for both designers and test engineers. This one-day seminar is intended for engineers and managers, either working in the areas of VLSI design and test, or intending to work in those areas. The course outlines the basic concepts in testing, defines terminology and discusses the commonly used practices. Included among these are testing costs, product quality and the design for test methodologies. Deep-submicron technologies have given rise to new problems of coupling effects, signal integrity, and increased leakage. How these affect testing is also discussed. The course outline is as follows:



### Part I. Introduction

1. VLSI test concepts and definitions
2. Test process and ATE
3. Test economics and product quality

### Part II. Digital Testing

1. Fault modeling
2. Logic and fault simulation
3. Combinational and sequential ATPG
4. Memory Test
5. Deep-submicron effects, signal integrity and leakage

### Part III. Analog Testing

1. Types of analog devices and their tests
2. DSP-based testing
3. Examples of analog testing
4. Analog built-in self test

### Part IV. Design for Testability (DFT)

1. Scan design
2. Built-in self-test (BIST)
3. Boundary scan
4. System on a chip (SOC) DFT

### Location

1762 Technology Drive, San Jose, CA

### About the Instructor:

**Dr. Agarwal** is the James J. Danaher Professor of Electrical and Computer Engineering at Auburn University, Alabama. Prior to that he has over 30 years of industry and university experience, working at Bell Labs, Murray Hill, NJ; Rutgers University, New Brunswick, NJ; TRW, Redondo Beach, CAEG&G, Albuquerque, NM; and ATI, Champaign, IL. His areas of work include VLSI testing, low-power design. He has published over 250 research paper and a book. Dr. Agarwal is well known authority and the top technical leader in VLSI testing area. He has won numerous awards in his career and a Fellow of IEEE and ACM.

### Tuition

Fee for the seminar is \$290 if registered and paid by Jan. 21, 2005, and \$350 if register after that. The registration fee includes:

- One day of instruction
- Seminar notes
- Lunch and refreshments

Seating is limited. Please register in advance.  
Email: [info@svtii.com](mailto:info@svtii.com)