



## Silicon Valley Technical Institute

1762 Technology Drive

San Jose, CA

Tel: 408-573-0100

Email: info@svtii.com

[www.svtii.com](http://www.svtii.com)

# ESD Design Methods for Nano-Scale CMOS Technologies

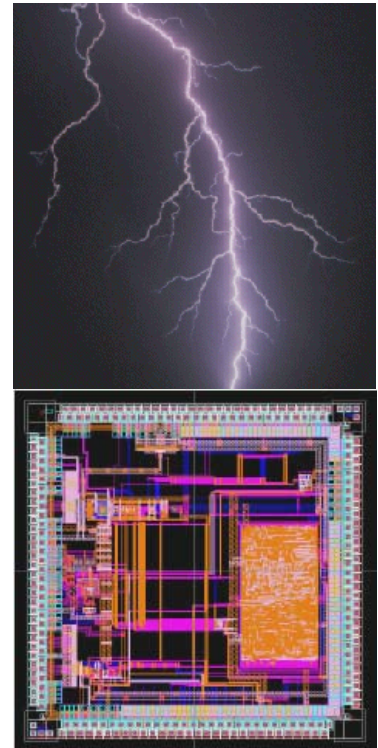
March 24, 2006

ESD failure is a major concern in the electronic industry. As IC designs migrate toward the VDSM regime, On-chip ESD protection circuits pose challenging design problems particularly for in deep submicron or nano-scale regime where the interactions between ESD protection networks and the circuits become critical.

This comprehensive ESD design seminar by a leading expert addresses various challenges from the sub-micron to the 65 nm CMOS technologies. The course will present the material with illustrative examples that form the necessary considerations for effective protection design. The attendee should gain enough knowledge and understanding for designing protection clamps for different technology and circuit performance demands.

This Seminar will cover,

- Basics of ESD Physics
- ESD Test Methods from Component HBM and CDM to System Level IEC
- Design of ESD Elements and Their Operation
- Advanced and Novel ESD Protection Devices
- Process Technology Scaling Impact on ESD Design
- Interaction Between ESD and Latchup
- ESD Simulation Methods
- New Developments in Circuit Designs and Constraints on ESD Design
- RF ESD Protection Strategy
- Voltage Tolerant and High Voltage ESD Designs
- System-on-Chip ESD Design
- IEC System Level ESD Design
- Product Level ESD Issues
- Methods for ESD Design Checks
- Upcoming New Technologies and Future of ESD
- Course Summary



### Schedule

#### Friday March 24, 2006

Check-in: 8:30 am –9:00 am

Lecture: 9:00 am - 4.00 pm

Lunch: noon-1:00 pm

### Tuition

Fee for the seminar is \$380. This includes:

- One day of instruction
- Seminar notes
- Lunch and refreshments

### Location

1762 Technology Drive, San Jose, CA

### Instructor

**Dr. Charvaka Duvvury** is a Texas Instruments Fellow and leading authority in design of ESD for Semiconductor Technology and devices. He has over 20 years experience and won numerous awards from ESD symposium, IPRS, and SRC. Dr. Duvvury has published more than 80 papers and presented many conference tutorials and courses. He is a senior IEEE member, a board member for ESD symposium and will be chairman for ESD symposium in coming Sept.2005.

Seating is limited. Please register in advance.

Register on-line at [www.svtii.com](http://www.svtii.com) or call

408-573-0100