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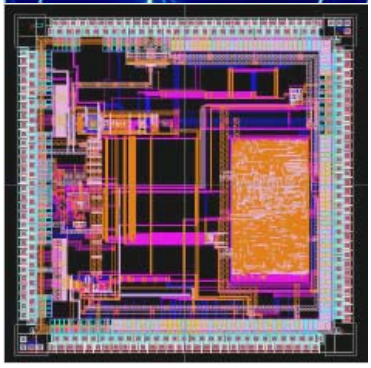
ESD Protection Design for Mixed-Signal/RF IC - A design perspective

Feb. 1, 2008
9:00am-5:00pm

ESD failure is a major concern in the electronic industry. As IC designs migrate toward the VDSM regime, On-chip ESD protection circuits pose challenging design problems particularly for mixed-signal and RF ICs, where the interactions between ESD protection networks and the circuits become critical.

This seminar starts with a review of ESD fundamentals including its origins, phenomena, operation, models, and different standards. Commonly used ESD protection structures and circuits will be discussed. Key issues on mixed-signal/RF ESD protection design, such as parasitic effects, ESD-circuit interactions, RF ESD protection measurement and evaluation techniques will be presented. Various RF ESD protection solutions will be described as well. In addition new CAD-based mixed-mode ESD simulation-design methodologies will be discussed. Finally research advances in full-chip ESD design verification CAD tool development are explored, and practical ESD design examples for industrial applications will be provided.



Part One: ESD Theory & Design

- ESD basics;
- ESD regulations & standards;
- ESD models, testers, & measurements;
- Trends in ESD specifications;
- Device level ESD protection design;
- Circuit level ESD protection design;
- Failure analysis & failure models;
- ESD protection and latch-up.

Part Two: Advanced ESD Design

- ESD stressing vs. TLP testing;
- ESD protection simulation - traditional;
- ESD protection design for VDSM ICs;
- Whole-chip ESD solutions;
- ESD protection for mixed-signal & RF ICs;
- ESD protection design for SOI & SiGe ICs;
- ESD protection interconnect design & design rules;
- Predictive mixed-mode ESD protection simulation-design methodology;
- ESD-to-circuit interactions;
- ESD protection design guidelines;
- Advanced ESD design examples;
- Full-chip ESD protection circuit design verification.
- 3D electro-thermal modeling for ESD protection devices.
- CAD for whole-chip ESD protection circuit design verification.
- Practical ESD protection circuit design examples.
- Low-parasitic RF ESD protection designs.
- RF ESD protection characterization.
- ESD-RF IC co-design methodology

Schedule

Check-in: 8:30 am –9:00 am
Lecture: 9:00 am - 5.00 pm
Lunch: noon-1:00 pm

Tuition

Fee for the seminar is **$370**. The fee includes:

- One day of instruction
- Seminar notes
- Certificate of attendance
- Lunch and refreshments

Location

1762 Technology Drive, Suite 227, San Jose, CA

Instructor

Dr. Albert Wang is a leading ESD design expert and Professor & Distinguished IEEE Lecturer in UC Riverside. He is the author of the book "On-Chip ESD Protection for Integrated Circuits" (Kluwer, 2002) and more than 110 papers in the field, and holds six U.S. patents. He is an Editor for the IEEE Electron Device Letters and an Associate Editor for the IEEE Transactions on Circuits and Systems I. He served as Guest Editor for the IEEE Journal of Solid-State Circuits, Guest Editor-in-Chief for the IEEE Transactions on Electron Devices and Associate Editor for the IEEE Transactions on Circuits and Systems II.

Seating is limited. Please register in advance.
Register on-line at www.svtii.com or call