



## Silicon Valley Technical Institute

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# DEVICE & INTERCONNECT RELIABILITY IN ADVANCED CMOS

Sept. 5, 2008

9am-4pm

As CMOS technology is scaled down, reliability of NMOS and PMOS transistors is affected by hot carrier effects (HCI), gate oxide degradation with time (TDDB) and interconnects degradation due to electro-migration effect (EM). Below 0.18 micron node new reliability issues emerge such as NBTI, PBTI, TDDB in high-k dielectrics, soft breakdowns and electro-migration failures in Cu/ Low K interconnect system.

This seminar provides a detailed understanding of reliability issues at the CMOS transistor and interconnects levels. The course explores physics behind various degradation mechanisms and methodology of lifetime evaluation. Impact on product reliability is explained. Circuit design rules to ensure adequate device and interconnect lifetime are explained. Emerging reliability failure modes in deep submicron, or nano-scale, regime are also explored. Current understanding of device physics, models and methods of lifetime evaluation of NBTI, ultra-thin oxide TDDB is covered. Impact of soft breakdowns, high-k dielectrics and EM in Cu/low-k systems is also discussed. The seminar covers:

- *Review of CMOS device physics and parameters*
- *Basics of traditional reliability evaluation and failure distributions*
- *Weibull statistics and practical application for lifetime projection*
- *Hot carrier degradation (HCI)*
- *Gate dielectric reliability (TDDB, QBD)*
- *Electro-migration (EM)*
- *Reliability design rule for circuit design*
- *Wafer Level FAB monitors*
- *Emerging reliability issues for deep sub-micron CMOS*
- *Ultra-thin oxide TDDB*
- *EM for Cu/Low K systems*
- *Hi k dielectric issues*

### Schedule

Check-in: 8:30 am –9:00 am

Lecture: 9:00 am - 4.00 pm

Lunch: noon-1:00 pm

### Tuition

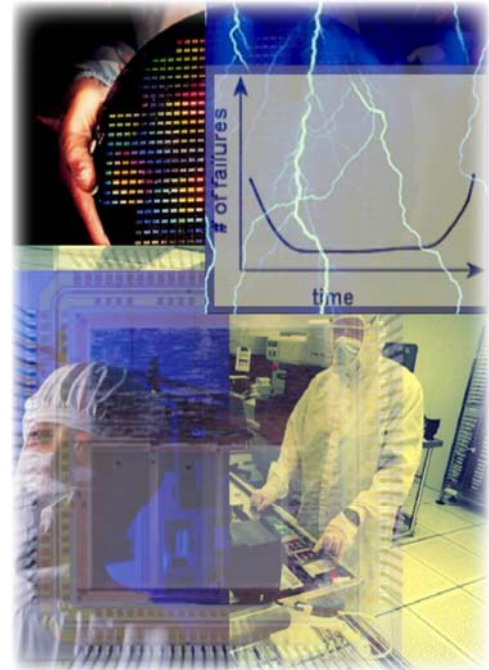
Fee for the seminar is **\$390**. Group discount is available for groups of 3 or larger. The registration fee includes:

- One day of instruction
- Seminar notes
- Certificate

Lunch and refreshments are included

### Location

1762 Technology Drive, Suite 227, San Jose, CA



### About the Instructor:

**Dr. Sunil Shabde** is a Silicon Industry veteran with over 25 years experience. Sunil has authored or co-authored 16 papers in the area of device physics and reliability in various technical journals such as IEEE Electron Device Transactions, IRPS, Solid State Electronics and Journal of Applied Physics. One significant contribution was the finding that ESD performance degrades due to LDD or a graded junction (1984 IRPS). He holds several patents and has received various awards. Dr. Shabde holds a Ph.D. in Electrical Engineering from Rice University and a senior IEEE Member.

Seating is limited.  
Please register in advance.  
Register on line at  
<http://www.svtii.com> or  
Call: 408-573-0100