



## Silicon Valley Technical Institute

1762 Technology Drive

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[www.svtii.com](http://www.svtii.com)

## ADVANCED SILICON TECHNOLOGY

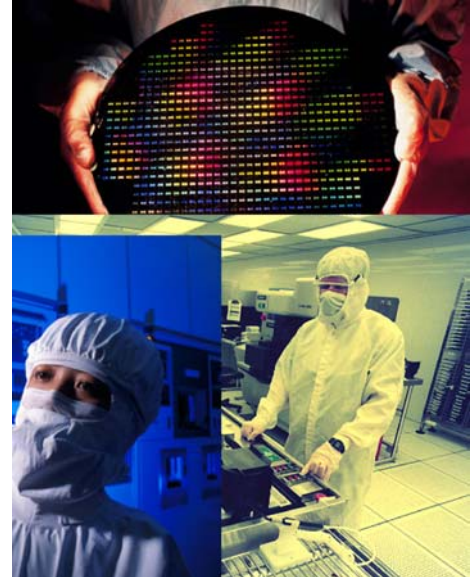
May 2, 2006

9am-5:30pm

### Description

This one day seminar will address the advances and practical aspects of device performance from 130nm node down to 90nm, and 65nm. During the seminar comprehensive details of 65 nm device manufacturing techniques, challenges, design for manufacturing (DFM) and Design for Reliability (DFR) issues will be addressed. A typical layout of an advanced 65 nm CMOS IC with embedded DRAM, Flash and CPU will be also explored. Requirements of these individual designs/technologies and their integrations on a single chip will be discussed. Amongst other topics to be addressed are the progression of Electrical Design rules and layout features relating to device performance as well as area savings from scaling, and other topics such as:

- **Fundamentals of CMOS device scaling**
- **ITRS roadmap and upcoming challenges**
- **90nm/65nm CMOS Devices and Process Flows**
- **Copper Dual Damascene**
- **High K dielectric as Gate Oxide stack**
- **Process Variability and impact on yield**



### Schedule

May 2, 2006

Check-in: 8:30 am –9:00 am

Lecture: 9:00 am - 5.30 pm

Lunch: noon-12:30 pm

### Tuition

Fee for the workshop is **\$360**. The registration fee includes:

- One day of instruction
- Certificate of attendance

(Lunch and refreshments are served at no extra cost)

### Location

1762 Technology Drive, Suite 227, San Jose, CA

### About the Instructor:

**Gian Sharma** is a hands-on Semiconductor Industry Process Veteran with 30 years experience. He has worked at Unisys, NASA, Chrysler Corp, Texas Instruments, Cypress Semiconductor, Xicor Inc; LSI Logic and SST as a Process Development technologist and Integration / R&D Engineer. He has interfaced regularly with wafer foundries in USA and Overseas on issues related to Process Development, & Process Transfers in to Manufacturing.

He has taught courses at Santa Clara University and is presently consulting in Silicon Valley. He received MSEE and MS Physics degrees from U of Nebraska, Lincoln and holds 5 US patents and a several publications.

Seating is limited. Please register in advance.

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